D: Remarks:

The amendment is made for the examiner's reconsideration of the claims in this application.

Again, the applicants contend that the references do not provide any on chip process for handling multiple bit failure detection, a fact that was true. The claims have been amended to clairify the on-chip diagnositic process but making changes that indicate the LSSD registers are used as diagnostic registers in the process claimed.

The applicants point out that the examiner has already found the limitation of N+1 in claim 1 was not in the art and that process is elaborated with this amendment. The references only show apparatus incapable of handing multiple failures on a chip diagnosis of fault, and do not show any on chip apparatus or process for handling multiple bit failure detection. They do not show the skipping process for reuse of chip circuitry, as the examiner has noted. The specific step by step method claimed is not shown by the references. To say that there is a programmable tester which can be created by a user and loaded in advance does not teach the invention. Those skilled in the art would recognize that the references cited by the examiner are external to the chip being tested and not on chip as in the claimed invention, and there is no teaching in any reference cited how to implement on chip testing at any level specified in the claims.

Both references cited by the examiner relate to external testers. In the case of Yasui 6594788 the device being tested is a memory under test 119.

Claim 1 specifies that the semiconductor circuit being tested is one "*having LSSD diagnostic registers on chip for a failing cell for desired handing of multiple failures on a failing chip for immediate scan-out off-chip at a level of assembly test after scan initialization of the LSSD diagnostic registers ~~of~~ on the semiconductor chip*". The memory under test 119 of Yasui does not meet this limitation.

Claim 1 further specifies that the test occurs in "*said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology*", something that can't occur in the memory under test 119 of Yasui.

In fact, the memory under test 119 of Yasui does not have any way of for providing: ***the desired failing chip handling on chip of multiple bit failure detection*** by any means at all.

Furthermore the claim 1 specifies that the on chip multiple bit failure detection occurs by:

providing data collection of a first failing cell in said LSSD diagnostic registers, and then skipping the collection of data up to a programmed amount to skip up to a subsequent failing cell.

Neither Yasui which tests MUT 119 nor Sato 5790559 which tests ECL semiconductor memory 206 provide this kind of data collection in LSSD diagnostic registers located on chip (indeed the elements

tested by Masui and Sato are different, and there is no apparent similarity gving rise to a desireability of combining elements of the two external testers and what would be the effect of a combination). There is no skipping data collection a programmed amount to skip up to a subsequent failing cell and no reuse of on chip logic. Neither Yasui nor Sato even talk about skipping up to a subsequent failing cell with their external testers. They can't test a semiconductor chip at any of the levels required by the claim, i.e. at any of the test levels of: an initial manufacturing wafer test, a module test, a system level test.

Indeed, they don't provide futher as specified in the claim 1, for:

recording the failure of a next failing cell recognized after said subsequent failing cell in said LSSD diagnostic registers while making reuse of logic including existing address registers for providing data synchronous with fail determination circuits for data collection used for collection of data of said first failing cell, and then

pinpointing an actual failure for said next failing cell using additional data collected by reuse of the logic for data collection used for collection of data of said first failing cell.

The applicants' contend that further, none of the steps set out in the dependent claims are shown in the art relied upon by the examiner. The applicants contend that each of the dependent claims is independently patentable, they not only incorporate each step of the independent claim which is not shown in the art, but also additional features which are not shown in the art.

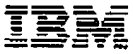
As stated in a Judge Rich decision, see Ryco In. v. Av-Bar Corp. 705 8 USPQ2d 1325 the Federal Circuit Court of Appeals stated that one question which must be answered in the affirmative to support a case of obviousness under 35 USC 103 is: "Do the elements of the reference perform the same function as those of the claim in issue?" Here the applicants contend that there is in the refernce no on chip failure detection which applies to more than one failure identification, after detection of a first failure, which can be found at **any of the test levels of: an initial manufacturing wafer test, a module test, a system level test.**

Indeed the references don't even provide any similar on chip tests, for all us off chip test devices, and don't provide the steps employed to achieve on chip testing by reuse of logic.

Critical differences, which include different functions, teachings away, and other criteria need to be recognized by the Patent Office as facts which will not support a conclusion of obviousness. These critical differences are one of the four factual inquiries under Graham pertinent to any obviousness query. Furthermore, obviousness cannot be established by combining the teaching of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive to supporting the combination. See: In re Bond 15 USPQ2d 1566, 1568 (FCCA 1990).

The abstract has now been reduced to less than 150 words in the previous amendment, and so the only remaining issue is whether the claims detail steps not shown by the art. That the applicants' contend is true.

If there is any further change that needs to be made, the applicant's attorney will be pleased if the examiner would



suggest it. Morning telephones are best for the undersigned. It is respectfully submitted that the application should be in final condition for allowance which is respectfully requested.

RESPECTFULLY SUBMITTED
(For the inventors)

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